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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,600	06/01/2001	Kevin B. Leigh	200301919-1	2616

22879 7590 07/17/2006

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 07/17/2006

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/872,600
Filing Date: June 01, 2001
Appellant(s): LEIGH ET AL.

David M. Hoffman (Reg. No 54,174)

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 14th of April 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments

All amendments have been entered

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection To Be Reviewed On Appeal.

The grounds of Rejection to be reviewed on appeal contained in the brief is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US Patent 5,706,447	Vivo	6-1998
US Patent 6,701,402	Alexandria et al.	3-2004
US Patent 6,072,943	Gasparik et al.	6-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-10, 12-21, 23-31, 35-41, 43-50, 52-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vivio (US Patent 5,706,447) in view of Alexandria (US Patent 6,701,402)

As per claims 1,13, Vivio discloses a method of switching control of a bus in a processor-based device, the method comprising the acts of:

- Electrically coupling a first bus controller to the bus; (col.4, lines 18-36)
- Generating a detection signal indicative of coupling of a second bus controller to the bus; and (col.4, lines 18-12)

Vivo discloses all the limitations as above except automatically isolating the first bus controller from the bus in response to the detection signal. However, Alexander discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claim 2, Vivio discloses the method comprising the act of terminating the first bus controller. (col.4, lines 18-62)

As per claim 3, Vivio discloses wherein the first bus controller is terminated response to detection of the detection signal. (col.4, lines 18-36)

As per claim 4, Vivio discloses wherein the bus comprises a plurality of traces disposed on a substrate, wherein the first bus controller is electrically coupled to a first segment of the plurality of traces, and wherein the second bus controller is electrically coupled to a second segment of the plurality of traces. (col.7, lines 5-48), wherein substrate equipped within connector)

As per claim 5, Vivio discloses the method comprising the act of terminating the second segment of the plurality of traces. (col.7, lines 5-48)

As per claim 6, Vivio discloses the method comprising the act of electrically removing terminating of the second segment of the plurality of traces in response to detection of the second bus controller. (col.7, lines 5-48)

As per claim 7, Vivio discloses wherein the first bus controller is disposed on a first substrate, and the second controller is disposed on a second substrate, the second substrate being coupled to the first substrate, and wherein the act of generating a detection signal comprises the act of transmitting the detection signal from the second substrate to the first substrate. (col.7, lines 5-56), fig.3, (col.4, lines 18-62)

As per claim 8, Vivio discloses wherein the first substrate comprises an expansion port, and a first end of the cable is connected to the expansion port. (col.6, lines 36-52), (claim 1, col.9, lines 35-48)

As per claims 9, 31,50, discloses wherein the bus comprises a SCSI bus.
As per claim 10, Vivio discloses wherein the first substrate and the second substrate each comprise a printed circuit board. (col.7, lines 5-56), fig.3, (col.4, lines 18-62)

As per claim 12, Vivio discloses wherein the act of electrically coupling comprises the act of coupling the first bus controller to the bus using a switch. (claim 1, col.9, lines 53-62)

As per claim 14, Vivio discloses wherein the act of detecting the presence of the second bus controller comprises the act of generating a detect signal when the second bus controller is electrically coupled to the bus. (col.4, lines 18-62)

As per claim 15, Vivio discloses wherein the act of automatically switching control of the bus comprises the acts of:

- Isolating the first bus controller from the bus; and (col.4, lines 18-62)
- Terminating the isolated first bus controller. (col.4, lines 18-62)

As per claims 16, 46, Vivio discloses the method comprising the act of terminating the bus proximate the first bus controller. (col.9, lines 42-44)

As per claim 17, Vivio discloses wherein the bus is terminated proximate the first bus controller in response to detecting the presence of the second bus controller. (col.4, lines 18-62)

As per claim 18, Vivio discloses wherein the second bus controller is disposed on a second substrate coupled to the first substrate. (col.7, lines 5-48), wherein substrate equipped within connector)

As per claim 19, Vivio discloses wherein the first substrate comprises an expansion port, and the method comprises the act of terminating the bus proximate the expansion port. (col.9, lines 42-44)

As per claim 20, Vivio discloses the method comprising the act of removing termination of the bus proximate expansion port in response to detecting the presence of the second bus controller. (col.4, lines 18-62)

As per claim 21, Vivio discloses the method of switching control of a bus in a low profile server, the low profile server comprising a first bus controller, a bus, and an isolation device, wherein the first bus controller is configured to control the bus, and wherein the isolation device is configured to isolate first bus controller from the bus(col.4, lines 18-62). Vivo discloses all the limitations as above except the method comprising the act of connecting a second bus controller to the bus to cause the isolation device to isolate the first bus controller from the bus. However, Alexander discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's

system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claims 23, 35, Vivio discloses a processor-based device, comprising:

- A processor; (fgi.1, 122)
- A memory coupled to the processor; and (fig.1, 124)
- A first substrate, comprising:
    - A bus disposed on the first substrate; (col.7, lines 5-48), wherein substrate equipped within connectors)
    - A first bus controller disposed on the first substrate, the first bus controller being coupled to the processor and the bus; and (col.4, lines 18-62)
    - An isolation device disposed on the first substrate, the isolation device being configured to couple the first bus controller to the bus,

Vivo discloses all the limitations as above except automatically isolating the first bus controller from the bus in response to the detection signal. However, Vivo discloses all the limitations as above except automatically isolating the first bus controller from the bus in response to the detection signal. However, Alexander discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claim 24, Vivio discloses the device comprising an expansion port disposed on the first substrate and coupled to the bus, wherein the expansion port is connectable to a second substrate, and wherein the second bus controller is disposed on the second substrate. (col.7, lines 5-48)

As per claim 25, Vivio discloses wherein the second bus controller is disposed on a second substrate, and the device comprises a cable having a first end and a second end, the first end being connectable to the first substrate, and the second end being connectable to the second substrate. (col.7, lines 5-48)

As per claim 26, Vivio discloses the device comprising a termination device disposed on the first substrate, the termination device being configured to terminate the bus proximate the expansion port when the second bus controller is not coupled to the bus. (col.9, lines 42-44), (col.7, lines 5-48)

As per claim 27, Vivio discloses the device comprising a termination device disposed on the first substrate, the termination device being configured to

terminate the bus proximate the first bus controller in response to detection of the second bus controller. (col.4, lines 3-62)

As per claims 28, 39, Vivio discloses wherein the isolation device comprises an electronic switch. (claim 1, col.9, lines 53-62)

As per claims 29, 40, Vivio discloses wherein the electronic switch comprises a transistor. (fig.3, col.7, lines 5-48)

As per claim 30, Vivio discloses wherein the processor and the memory are disposed on the first substrate. (Fig.5, 120 i/o)

As per claim 36, Vivio discloses the board comprising a termination device disposed on the substrate and configured to terminate the first bus controller in response to detection of the second bus controller coupled to the bus. (col.4, lines 18-62)

As per claim 37, Vivio discloses the board comprising an expansion port disposed on the substrate and coupled to the bus, wherein the second bus controller is coupled to the bus via the expansion port. (col.7, lines 5-48)

As per claim 38, Vivio discloses the board comprising a termination device disposed on the substrate and configured to terminate the bus proximate the expansion port when the second bus controller is not coupled to the bus via the expansion port. (col.7, lines 5-48)

As per claim 41, Vivio discloses the printed circuited board comprising:

- A memory disposed on the substrate; and (fig.5, 120 I/O)
- A processor disposed on the substrate, the processor being coupled to the memory and to the first bus controller.(fig.5, 120 I/O)

As per claim 44, Vivio discloses a method of manufacturing a device for switching control of a bus in a processor-based device, the method comprising the acts of:

- Providing a bus disposed on a substrate; (fig.5, connector 210, 510)
- Connecting an expansion port to the bus, the expansion port being configured for connection to a second bus controller; (col.7, lines 5-48)
- Disposing an isolation device on the substrate, the isolation device being connected to the bus; and (col.7, lines 5-48)
- Disposing a first bus controller on the substrate, the first bus controller being connected the isolation device (col.4, lines 18-62), (col.7, lines 5-48)

Vivo discloses all the limitations as above except the isolation device being configured to isolate the first bus controller from the bus when a second bus controller is connected to the expansion port. However, Alexander

discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claim 45, Vivio discloses the method comprising the act of disposing a termination device on the substrate, the termination device being connected to the bus. (col.4, lines 18-62)

As per claim 47, Vivio discloses the method wherein the termination device is configured to terminate the first bus controller when the second bus controller is connected to the expansion port. (col.7, lines 5-48)

As per claim 48, Vivio discloses wherein the termination device is connected to the bus proximate the expansion port. (col.9, lines 42-44)

As per claim 49, Vivio discloses wherein the termination device is configured to terminate the bus proximate the expansion port when the second bus controller is not connected to the expansion port. (col.9, lines 42-44) (col.7, lines 5-48)

As per claim 52, Vivio discloses a method of manufacturing an expansion card connectable to system controller board having a system bus controller configured to control the bus, and having an isolation device configured to isolate the system bus controller from the bus in response to a detect signal, the method comprising the acts of:

- Disposing an expansion us controller on a substrate, the expansion bus controller being configured to control a bus; (col.4, lines 18-62)
- Disposing a detect signal generator on the substrate; (col.7, lines 5-48)
- Connecting the detect signal generator to the first expansion connector; and (col.7, lines 5-48)
- Disposing a first expansion connector on the substrate, the first expansion connector connected to the expansion bus controller and the detect signal generator, (col.7, lines 5-48)
- Wherein the first expansion connector is configured to couple with a cable, the cable having a first end connectable to the first expansion connector and a second end connectable to a system controller board, and (fig.3, and fig.5), (col.7, lines 5-48)

- Wherein the detect signal generator is configured to generate a detect signal detectable at the second end of the cable when the expansion board is connected to the system board via the cable. (fig.3, and fig.5), (col.7, lines 5-48)

Vivo discloses all the limitations as above except wherein the isolation device is configured to isolate the system bus controller from the bus in response to the detect signal. However, Alexander discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claim 53, Vivio discloses a method of switching between a first device and a second device connectable to a communications medium in a processor-based device, the method comprising the acts of:

- Electrically coupling a first device to the communications medium; (col.4, lines 58-62)

- Generating a detection signal indicative of coupling of a second device to the communications medium; and (col.4, lines 18-62)

Vivo discloses all the limitations as above except automatically isolating the first device from the communications medium in response to the detection signal. However, Alexander discloses when controller is given master access to bus, controller is the only master communicating with the disk controller, other masters connected to bus are not communicate with disk controller until controller relinquishes master access to bus. (col.3, lines 7-13)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Alexander's teaching into Vivo's system so as to facilitate the use of preexisting controller in a host for a peripheral device connected to the host. (col.1, lines 44-46)

As per claim 54, Vivio discloses wherein the communications medium comprises a point-to-point interconnect. (col.7, lines 5-48)

As per claim 55, Vivio discloses wherein the communications medium comprises shared bus. (fig.5, bus 120)

Claims 11,22, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vivio (US Patent 5,706,447) in view of Alexandria (US Patent 6,701,402), and further in view of Applicant Admitted Prior Art

As per claims 11 and 34, Vivio discloses all the limitations as above except a low profile server. However Applicant admitted prior art discloses designs of low profiles servers which have a reduced height between the base and top of the chassis. (page 2, lines 23-24)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate AAPA's teaching into Yanagisawa's method so as to reduce the height.

As per claim 22, Vivio discloses wherein the first bus controller is disposed on a first substrate, and wherein the second bus controller is disposed on a second substrate, and the act of connecting the second bus controller to the bus comprises the acts of:

- Disposing a cable, the cable comprising a first end and a second end; (col.7, lines 5-48, fig.4)
- Connecting the first end of the cable to the first substrate; and (col.7, lines 5-48, switch 222)
- Connecting the second end of the cable to the second substrate. (col.7, lines 4-48, fig.5)

Yanagisawa discloses all the limitations as above except a low profile server. However Applicant admitted prior art discloses designs of low profiles servers which have a reduced height between the base and top of the chassis. (page 2, lines 23-24)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate AAPA's teaching into Yanagisawa's method so as to reduce the height.

Claims 32-34, 42, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vivio (US Patent 5,706,447) in view of Alexandria (US Patent 6,701,402) and further in view of Gasparik et al. (US Patent 6,072,943)

Vivio discloses all the limitations as above except a SCSI device connectable/operatable to the SCSI bus. However, Gasparik discloses the SCSI bus is designed to connect independent devices, such as a SCSI bus 20 couples first SCSI device 12 to SCSI 14 which provides a communication path between the device 12 and 14. (col.3, lines 52-67)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Gasparik's teaching into Vivio's system so as to provide each SCSI device with termination capabilities. (col.2, lines 11-15)

(10) Response to Argument

Appellants' brief filed on 4/19/06 have been fully considered but does not place the application in condition for allowance.

In section A, item 1, Appellants set forth the criteria for a *prima facia* case of obviousness, but fail to specifically point to any deficiencies with respect the rejections. Accordingly, the examiner makes no response to this portion of appellants' arguments.

In section A, item 2, with respect to claims 1, 21, 23, 35, 44, 52, and 53, appellants have argued that Alexander, III et al. fail to teach "a method or device for automatically isolating a first bus controller from the bus in response to a second bus controller being coupled to the bus (or in response to the generation of a detection signal indicating that a second controller has been coupled to the bus)". In particular, appellants argue that in Alexander, III et al. the first bus control is not **isolated** from the bus. The examiner respectfully disagrees.

Examination of the specification of the instant application reveals no specific definition of the term "isolated". Accordingly, this term is given its broadest reasonable interpretation in accordance with the specification. On page 11 of the specification the term is used in the following context:

> If used, the controller terminator 76 may be a single-ended terminator to provide appropriate termination for certain control signal lines on the ROC 42, thus preventing improper operation or malfunction of the operating system due to inquiries from other application to the SCSI bus through he ROC 42 when isolated from the SCSI bus segment 58.

This usage implies that "isolation" prevents improper operation or malfunction of the operating system due to inquiries from other applications. In Alexander, III et al. when the PCI bus controller gives control to one of the masters, the other masters are prevented from communicating with the disk controller and are thus "isolated" from it. Alexander, III et al. further make specific mention in the abstract that the purpose of this "isolation" is to avoid data collisions, data loss and possibly system failure as required by appellant's use of this term.

Appellants further argue that in Alexander, III et al. the isolation does not occur "in response to the detection signal" as claimed. The examiner agrees; however, Alexander, III et al. was not relied upon for this limitation. The primary reference to Vivio discloses the generation of a detection signal indicative of coupling of a second bus controller to the bus (col. 4, l. 49). Vivio further discloses switching control based on the detection signal. When the teachings of Alexander, III et al. are applied to the system disclosed by Vivio the result is a system wherein isolation takes place in response to the detection signal as claimed.

Appellants do not argue claims 21, 23, 35, 44, 52, and 53 separately, but only based on their dependence on claim 1. Accordingly, the rejection of these claims is maintained.

In section A, item 3, appellants have reiterated the above arguments against the rejection of claim 13. As no new arguments are presented for claim 13, the examiner respectfully directs the Administrative Patent Judges' attention to the response above.

In section A, item 4, appellants argue that modification of the Vivio reference in view of the teachings of Alexander, III et al. would render the Vivio reference unsatisfactory for its intended purpose. Specifically, appellants argue that Vivio is directed to a system that facilitates the addition of a second processor to a computer system that is intended to work in conjunction with the first processor and not take control of the bus 120. The examiner respectfully disagrees. The Vivio reference is not limited to embodiments wherein processors operate in conjunction with one another. Vivio specifically contemplates the use of different microprocessors (col. 6., lines 23-

26), which may or may not be designed to operate in conjunction. Accordingly, isolating these processors in accordance with the teachings of Alexander, III et al. does not render Vivio unsatisfactory for its intended purpose.

In section A, item 5, appellants re-characterize the argument above in terms of changing the operating principle of Vivio. Again, appellants are giving too narrow of an interpretation of Vivio. While Vivio contemplates systems with dual processors, its disclosure is not limited to only such systems. As the title of Vivio states, Vivio is directed to a System For Automatic Reconfiguration Termination To Multi-processor Bus Without Added Expense Of Removable Termination Module and is not limited to dual processors as appellants assert.

In section A, item 6, appellants again re-characterize the argument of items 4 and 5, this time as "teaching away". As discussed above, there is nothing in Vivio, which prohibits "isolation" of the processors as taught by Alexander, III et al. Appellants' arguments are not based on a fair reading of Alexander, III et al.

In section B, item 1, appellants contest the rejection of claims 11, 22, and 34 based on their dependency from claims 1, 21, and 23, respectively. As no new arguments are presented, the examiner maintains the rejection of these claims.

In section B, item 2, appellants contest the rejection of claims 32-34 (sic), 42, and 51 based on their dependency from claims 23, 35 and 44, respectively. As no new arguments are presented, the examiner maintains the rejection of these claims.

(11) Related proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the Examiner in the Related Appeals and Interferences section of this Examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully Submitted,

Cel/
July 3, 2006
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